Multiplexing single electron transistors for application in scalable solid-state quantum computing

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Single electron transistors (SETs) are nanoscale electrometers of unprecedented sensitivity, and as such have been proposed as readout devices in a number of quantum computer architectures. The authors show that the functionality of a standard SET can be multiplexed so as to operate as both readout device and control gate for solid-state qubit systems based on charge localization and spin-charge transduction. Such multiplexing offers new possibilities for gate density reduction in nanoscale devices, and may therefore play a role in scalable quantum computer architectures.


The single electron transistor (SET) is a device that can act as an exquisitely sensitive electrometer. This sensitivity derives from precise control of the absolute charge state of a small metallic island, coupled via tunnel junctions to macroscopic leads. Since Fulton and Dolan’s initial experiments, SETs have been suggested for a diverse range of applications, from elements for classical logic to single-photon detectors. SETs are commonly suggested as readout mechanisms for quantum scale devices such as cellular automata and quantum computers (QCs), either via direct sensing of charge qubits or of spin qubits after an initial spin to charge transduction process, and this sensitivity has been routinely proven, e.g., Refs. 15 and 16.

Merely showing that SETs have the required sensitivity for qubit readout is not, however, sufficient for the development of a scalable quantum computer architecture. Of principle concern in this letter is the requirement for minimal gate density in a scalable quantum computer. Although we explicitly consider a charge-based double quantum dot (QD) qubit system in our model, the results are applicable to spin qubits in that the process of spin-charge transduction requires a similar gate control and a charge localized readout. The qubit states correspond to the localization of a shared electron between one of two QDs. The circuit model for this SET-2QD system is shown in Fig. 1(c).

We work in the steady state regime where the current through the SET is modeled via energy minimization arguments of the entire system, following the orthodox theory of electromagnetic phenomena.

FIG. 1. (a) Example of conventional single electron transistor (SET) design. The large footprint will present difficulties in a scalable quantum computer. (Image taken from Ref. 18.) (b) Schematic of multiplexed SETs designed for minimizing gate density in a scalable quantum computer. (c) Circuit diagram for the SET coupled to two quantum dot (SET-2QD) system. The SET consists of three continuously variable voltage sources (source, drain, and gate), coupled to an isolated island. The source and drain are connected to the island by tunnel junctions, allowing for current flow through the SET. Isolated regions in which effects due to electron occupation number are critical have been indicated with boxes.

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The total charge is expressed as \( \mathbf{Q} = \mathbf{\tilde{Q}} - n \mathbf{q}_e \), where \( \mathbf{n} \) is a vector containing the excess electrons on each isolated region. \( C_E \) describes the cross capacitances of the QDs and the island and is given by

\[
C_E = \begin{bmatrix}
C_{22} & -C_{11} & -C_{12} \\
-C_{11} & C_{11} & -C_{12} \\
-C_{21} & -C_{21} & C_{11}
\end{bmatrix},
\]

where \( C_{22} \) is the total capacitance of the \( \alpha \) isolated region to all other objects in the system ( \( C_{22} = \sum_{\alpha \neq \beta} C_{\alpha \beta} \) ). The above relations allow the determination of the current through the SET for the full SET-2QD system for any voltage on the electrodes. We calculate the current based on a standard master equation approach and the materials and geometry of the SET design.

The present limit to detectable SET currents is in the femtoampere regime.\(^{23}\) We choose to scale the geometry of a SET in Fig. 1(b) to produce a minimal footprint such that the electrodes’ height and width are 10 nm, and the tunnel junction barriers are 3 nm thick, while remaining above this limit. Such a scaling is conducive to current estimates of the size and spacing required for atomic-scale solid-state qubits in silicon, indicating that the structure of Fig. 1(b) is compatible with future scalable quantum computers. Reducing the resistance of the SET tunnel junctions will provide a commensurate increase in current without affecting the conclusions of this letter, for example, by using devices fabricated with overlapping junctions obtained by standard shadow mask evaporation techniques. Furthermore, an alternative fabrication method based on the use of scanning tunneling microscopes\(^{23}\) indicates that structures of this scale are achievable.

The capacitive coupling between the leads of the SET (e.g., source and gate) may be problematic in this structure due to the slowing of the rise time \( (\approx RC) \) of the voltages on the leads for qubit control. Our finite element modeling of the scaled geometry of Fig. 1(b) determines these cross-lead capacitances to be of the order of 10 aF. The operation speed for qubit control can therefore be maintained at an acceptable picosecond rise time for the voltages on the leads, so long as the resistance in the leads is of the order of kilohms. For the SET to perform readout of the qubit, the operation will need to be performed such that the variation in the current through the SET for the qubit being in each of its two states is a maximum. For control, the SET will need to be operated in regions where there is no current passing through the SET.

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The lines A, B, and C in Fig. 3 (and all lines parallel to them) are lines of constant-\(Q\)-QD potential difference, with corresponding potential well diagrams shown. The paths were calculated using Eq. (2), noting that constant po...
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FIG. 3. Magnitude of the difference in current through SET for a single electron occupying QD1 or QD2 ($\Delta I_{32}$) in Fig. 1(g), normalized to the maximum current through the device. Units are dimensionless: $V^g_{c}=(C_{c}+V_{g})(C_{d}+C_{id})/2e$. Following the path 1-2-3-4, the SET can be used to both readout and control the state of the qubit.